CDF Run IIb Silicon: Stave design and testing

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***Abstract*—The various generations of Silicon Vertex Detectors (*SVX, SVX', SVXII*) for CDF have been shown to be a fundamental tool for heavy flavor tagging via secondary vertex detection at the Fermilab Tevatron. The CDF RunIIb Silicon Vertex Detector (*SVXIIb*) has been designed to be a radiation tolerant replacement for the currently installed *SVXII* as it could not survive the anticipated Tevatron luminosity for the RunIIb. One major difference with respect to the current silicon detector is the employment of a single mechanically and electrically independent element used throughout the detector. This element, called *stave*, carries six single sided silicon sensors on each side and is built using high thermally conductive carbon fiber skins on a foam core with a built-in cooling channel. A Kapton bus cable carries power and data/control signals underneath the silicon sensors on each side of the stave. Sensors are readout in pairs via a ceramic hybrid glued on the sensor itself and equipped with four new SVX4 chips. This new design concept leads to a very compact mechanical and electrical detecting unit, allowing streamline production and ease of testing and installation. A description of the design and mechanical performance of the stave is given. We also present here results on the electrical performance obtained using prototype staves.**

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I. INTRODUCTION

THE CDF Run IIb silicon detector (SVXIIb) [1,2] is designed to be a radiation tolerant replacement for the current 5-layer SVXII [3] and Beam-pipe layer (L00) [4] detectors. The design of SVXIIb is optimized for Higgs and new particle searches while also being affordable, robust, and simple to construct and operate. To minimize the development time, the design of SVXIIb makes use of existing technologies and specific CDF infrastructure to the largest extent possible.

The new detector is divided into two barrels covering a total of about 1.2 m along the beam direction (the CDF luminous region is about 35cm), with 6 active layers (full phi coverage for each layer) spanning radically from 2.1 cm up to 18 cm from the beam line. Staves populate layers 1 through 5 for a total of 180, while the innermost layer (layer 0) is totally different in concept and follows the design of the previous L00. The layout of the SVXIIb is shown in Fig. 1. Each stave has single-sided sensors on both sides of a carbon fiber/foam mechanical structure with embedded cooling tubes.

For the SVXIIb detector, a new radiation hard SVX readout chip, called SVX4 [5], has been designed on 0.25 microns

CMOS technology by a collaboration between LBNL, University of Padova and Fermilab and fabricated at TSMC.

There are only 2 designs of single sided silicon microstrip sensors for the outer 5 layers: axial and stereo. The strips on the stereo sensors have a 1.2 degree angle with respect to the axial direction. Staves on layers 1 and 5 have axial sensors on both sides, while staves for layers 2, 3 and 4 are instrumented with both axial and stereo sensors on opposite sides. As a tracking device SVXIIb works in conjunction with ISL [6] (1 silicon layer in the central region and 2 layers for pseudorapidity between 1 and 2) and the outer tracking chamber [7] (COT). The combination of these three detectors provides excellent track reconstruction efficiency and purity in the very dense track environment expected for the high luminosity RunIIb at the Tevatron. The silicon sensors are made at HPK on 6", 320 μm thick wafers with strip pitch of 75 μm for the axial and 80 μm for stereo sensors. The depletion voltage is between 100 V and 200 V and the sensors good design and quality allows operation in excess of 500V. Studies on these sensors also after heavy irradiation confirm good quality and operability even after fluencies corresponding to ~20 fb^{-1} of data collected at the Tevatron.

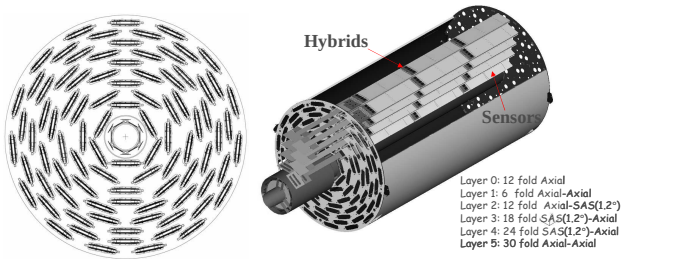

Fig. 1. Outer bulk-head end-view (left) and a 3-D layout of one barrel (right) showing stave population of SVXIIb barrel volume.

II. Stave Design Overview

The new and unique aspect of the stave design consists in the fact that active silicon, power distribution, data and control cables and cooling are integral part of the mechanical support structure. Using the same stave design for over 90% of the detector volume has the advantage of very few types of components, fewer construction fixtures and streamlined production processes, fast construction and reduced costs. Another important feature of this design is that the staves are essentially interchangeable and the detector could be de-scoped with extreme ease.

Silicon sensors, bus cables, readout hybrids and Mini Port-card are all the electrically active components populating both sides (except for the Mini Port-card) of the stave mechanical support structure. Fig. 2 gives a break out view of the stave components. Six axial sensors are mounted on one side and six axial or stereo sensors are mounted on the other side. As mentioned in the introduction, the innermost and outermost layers are instrumented with double axial staves facilitating track linkage with the outer tracking system and allowing for fast pattern recognition algorithms. The three intermediate axial/stereo layers provide 3-dimentional track information for vertex reconstruction and stand alone tracking (especially important in the forward region where no COT information is available).

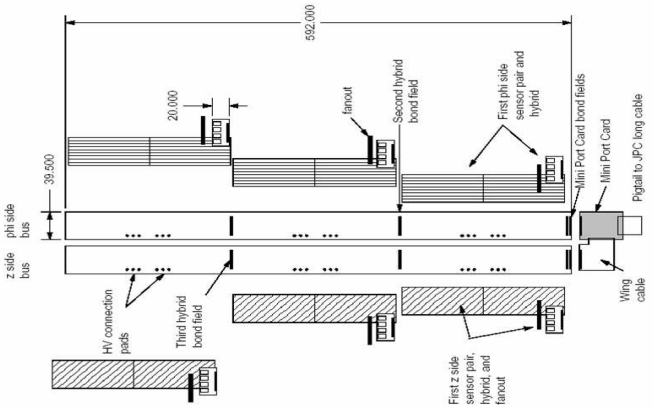

Fig. 2. The components and structure of a stave.

III. Mechanical Overview of Stave

The total length of a stave is 66 cm. The core of a stave is made by 2 high conductivity carbon fiber composite skins[‡] on a foam core with a built-in cooling tube. The design aims for a light and rigid structure. Two copper on kapton bus cables (190 μm thick), used for data, controls and power distribution, are further laminated on the carbon fiber skins. Mini Port Card and six silicon modules are finally precisely glued to the core assembly and wire bonded down to the bus cable. A gap of 3 mm between modules and openings in the bus cable shield expose wirebonding pads for connection to the hybrids and Mini Port Card..

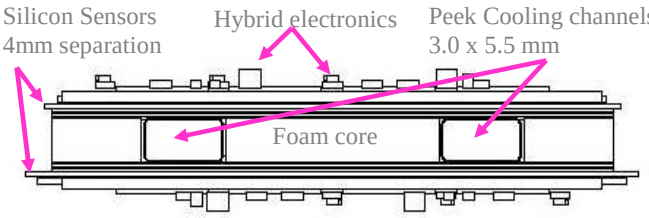

Fig. 3. A view of cross-section on stave structure and material.

A. *Mechanical Support*

The stave position is registered by precision holes and slots in aluminum inserts glued into each end of the stave core. These fit onto precisely located pins protruding from the inner and outer bulkheads. With this design we achieve an average module alignment with respect to the stave axis of 20 μrad. The total alignment precision within a barrel is expected to be better than 150 μrad.

The gravitational sag over the total length of the stave is less than 150 μm which is in agreement with the finite element analysis (Fig.4 left). The relevant alignment requirement for this coordinate is however the radial deviation within a module for which we achieve an average value of 100 μm.

[‡]4 plies of K13C2U oriented 0/90/90/0 for a total thickness of 250 um

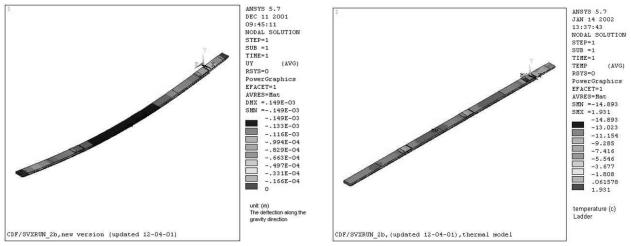

Fig. 4. (Left) Finite element analysis of stave structure under gravity. (Right) Stave temperature distribution assuming coolant temperature of -15 C.

B. Stave Cooling

To prolong the lifetime of the detector in the high radiation environment, silicon sensors are required to operate at cold temperature. The innermost layers receive the largest radiation dose and thus have the tightest temperature specification (-5C at Layer 1) while the outermost layer could operate up to 15C as the radiation scale as $\sim r^{-1.5}$ in the CDF environment [8]. Good thermal coupling between the sensors and the cooling system is important to achieve these values. The expected heat generated by a stave is about 18 W including 9.6 W from the 24 SVX4 readout chips, 4.2 W from convection, 2.5 W from the Mini Port Card, and 1.6 W from leakage current assuming a dose equivalent to an integrated luminosity of 30 fb^{-1}.

The core of a stave contains a built-in U-shaped cooling tube. The cooling channel is formed using a 0.1mm wall thickness polyetheretherketone (PEEK) plastic tube, selected for its radiation tolerant properties. A finite element thermal model has been developed to study the temperature trends on the stave. Assuming a coolant temperature of –15C[§], the highest temperature spot on the silicon is –2.9C, underneath the readout hybrid. The maximum strip temperature (averaged over the strip volume) is about -10C on the axial side and -4C on the stereo side.

The cooling system will be operating below atmospheric pressure in the detector region to avoid leaking into the active volume. There will also be a gas system providing a continuous cooled gas flow of nitrogen to the detector volume. This dry gas keeps the silicon volume slightly over atmospheric pressure and prevents condensation.

C. Stave Material

Given the detector design, the stave material represents nearly all material inside the tracking volume. Therefore special attention has been given to minimize the stave material budget achieving a total of 1.95% radiation length (X_0) on average for perpendicular tracks. Contributions to the total come from: 37% silicon, 16% hybrids, 16% bus cables, and 31% support structure and cooling. This achievement is especially significant when compared to the SVXII total material budget which is about the same in spite of the employment of double sided silicon sensors in the latter and the higher level of radiation tolerance of the former. The extra silicon material and cooling capability in SVXIIb is compensated by a smaller hybrid design and the positioning of the Mini Port-card, service cables and pipes at the end of the stave, outside the tracking volume.

IV. STAVE READOUT ELECTRONICS

From a data acquisition point of view each stave constitutes a single readout unit. Data is read out serially along the stave starting from the module far from the Mini Port Card on the axial side and finishing with the module closest to the Mini Port Card on the opposite side (whether axial or stereo) of the stave. The Mini Port-card at the end of stave connects bus cables on both sides for power distribution, readout processing and bidirectional data control. An important feature of the readout scheme (common to all CDF silicon readout chips) is the capability of reading out only channels above a certain predetermined pedestal value (sparse readout) and optionally their neighbors, hence dramatically reducing the readout time and data size.

One of the major challenges of the stave design is given by its performance in terms of dead-timeless operation. This is due to the fact that the bus cable, running directly underneath the active silicon sensors is constantly occupied by control and clock signals going back and forth to the SVX4 chips while the front end is acquiring data.

A. SVX4 chip

The SVX4 chip is designed and fabricated on 0.25 μm CMOS process and inherently radiation hard. It contains 128 parallel charge integration channels each with and integrated 8-bit ADC. The chip is designed to run in a dead-timeless mode: the front-end (analog) part can run in parallel with the back-end (digital) part. For each channel, there are 46 pipeline cells to store the data. The pipeline depth covers the CDF Level 1 trigger latency and allows for up to 4 physics events to be held for further digitization and readout. The chip operates at +2.5V.

The other important features of SVX4 chips are:

1) Maximum interaction rate of 132 ns (i.e. time between collisions).
2) Optimized for input capacitive load between 10 to 40 pF.
3) Built-in charge injection circuit for preamp calibration on a channel by channel basis.
4) Sparsified readout (channels above threshold and, optionally, neighbors)
5) A programmable shunt circuit to exclude faulty strips from saturating the preamp and affecting performance of adjacent strips.
6) Real time event-by-event pedestal subtraction circuit to effectively eliminate common mode noise.

All above features are perfectly working and from an operational point of view especially important is feature 5 (this is a new feature of the SVX4 chip) in the above list, as leaky strips can be effectively 'killed' on-line with no consequences to neighboring strips. The noise of an SVX4 chip in ENC is about 400 + 40 * pF. The dynamic range of the amplifier is 200fC.

[§] 43% by weight of ethylene glycol in water.

B. Hybrid

The SVXIIb hybrid used on the stave is a Beryllium Oxide (BeO) substrate circuit board with gold conductors. There is just one hybrid design for all staves. Each carries four SVX4 chips. The BeO substrate has the advantage of low mass and good thermal conductivity. By using 100/100 μm trace/space and 125 μm via technology we reduced considerably the size of this hybrid with respect to the previous version for the SVXII. Ceramic pitch adapters are used to match the bond field of the hybrid to the sensors. Hybrids are extensively tested and burned-in before been used on modules. Since there is no readout cable on the hybrid, multiple bondable pads are provided for use with a small PCB for testing purposes (Fig. 5, 6).

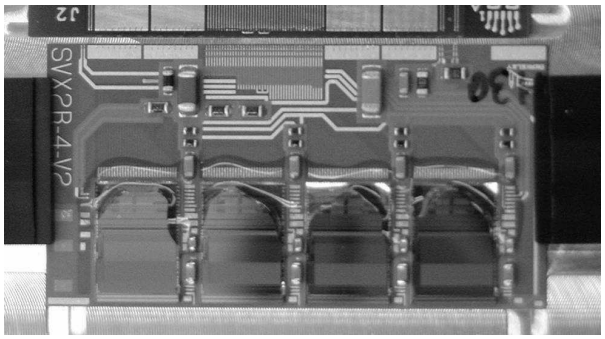

Fig. 5. A BeO hybrid carries 4 SVX4 chips. Notice how all wirebonds are encapsulated for protection except for the SVX4 chip inputs. Notice also the presence of the testing PCB on the top of the figure and the multiple wirebonding pads.

C. Mini Port-card

The Mini Port-card (MPC) also uses a BeO substrate. There are five transceiver chips and by-passing and termination components mounted on the MPC. Two flex cables are used to connect the MPC to the upper DAQ system, one for data and control signals and one for power. An additional flex cable is bent around the side of the stave and glued on to the carbon fiber opposite to the MPC. This flex cable (called wing) is used to connect MPC with the bus cable on the back side of the stave.

All the communication signals, like clock and control signals, to the DAQ use LVDS (low voltage differential signal) protocol. All signals are regenerated at the MPC and sent to the chips on the hybrids. Some signals will be transformed from LVDS to single ended signals for the chips. Some of the data bus lines are bi-directional, and the differential drivers on the MPC regenerate the signal in both directions.

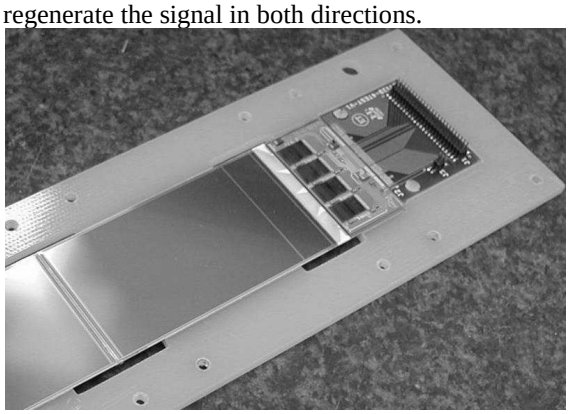

Fig. 6. A picture of a module. Two silicon sensors are wire bonded and held by a G10 frame. One side of the sensor is bonded to a pitch adapter which connects to the SVX4 chips on hybrid.

D. Bus cable

The bus cable is a flexible etched laminate of kapton, copper and aluminum foil. The cables are laminated to the carbon fiber surface of the stave. The single-sided silicon sensors are glued on top of the cable. There are gaps, about 3mm wide, at the location between modules to allow wire bonds from the hybrids to the bus lines. Bus traces are 75 μm wide with 100 μm space and paired if they are used for differential signal transmission. Each pair is separated by a 150 μm gap. Power and ground traces are wider to avoid voltage drop.

A 25 μm thick aluminum shield separates the bus traces from the sensors back plane. This shield is crucial to avoid pickup noise into the sensors. The best ground configuration for the shield was found to have it grounded to the closest analog ground on the hybrid. The connection should be solid to have small impedance and inductance. The impedance of the bus depends on the geometry and kapton thickness between bus lines and carbon fiber below and aluminum shield above. The measured value is at 75 ohms.

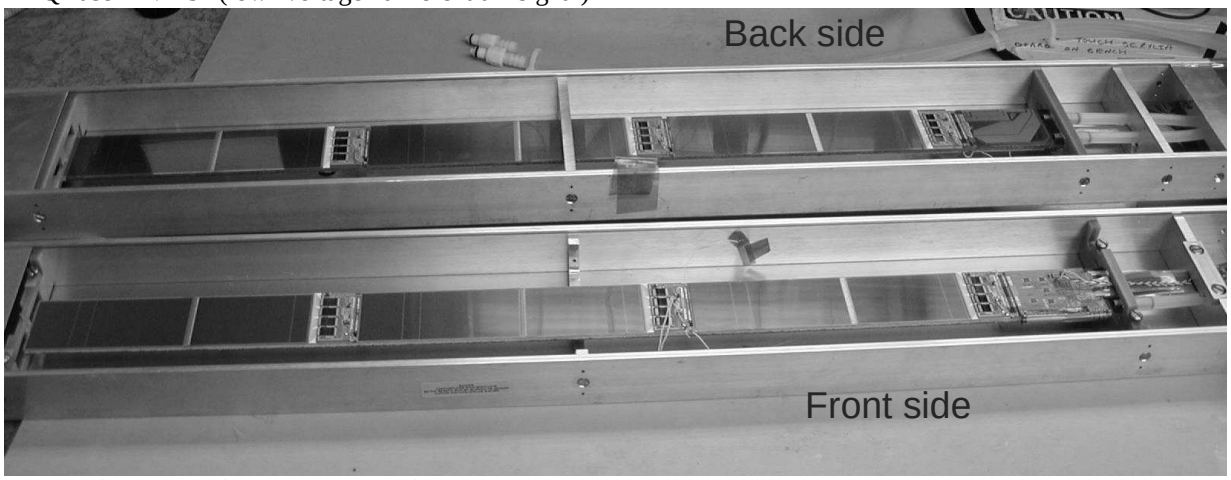

Fig. 7. A picture of staves. Both front and back sides of staves are shown.

IV. STAVE ELECTRICAL TESTING

All components undergo a thorough testing before been installed on a stave. Sensors are individually tested at HPK and retested on a sample basis at University of Tsukuba, University of New Mexico and Purdue University; SVX4 chips are probed on their wafer at Fermilab before dicing; hybrids are assembled and tested at LBNL and burned-in at U.C. Davis for at least three days before shipping to Fermilab. Quality assurance and control on individual parts is a priority to ensure good performance of the final product [9].

A. Chips/Hybrids/Modules testing

Pedestal, noise, and differential noise (dnoise, i.e. common mode noise suppressed) distributions are the primary tools to determine good quality of chips, hybrids and modules. Fig. 8 (top) shows pedestal and noise distributions for a single SVX4 chip with capacitors loaded for several preamp input values. The increased noise with input capacitive load is as expected (Fig. 8, bottom).

Fig. 9 shows pedestal distribution with charge injection on a prototype hybrid. Other common testing tools such as gain scans, bandwidth scans , pipe cell noise and pedestal scans etc. are routinely performed.

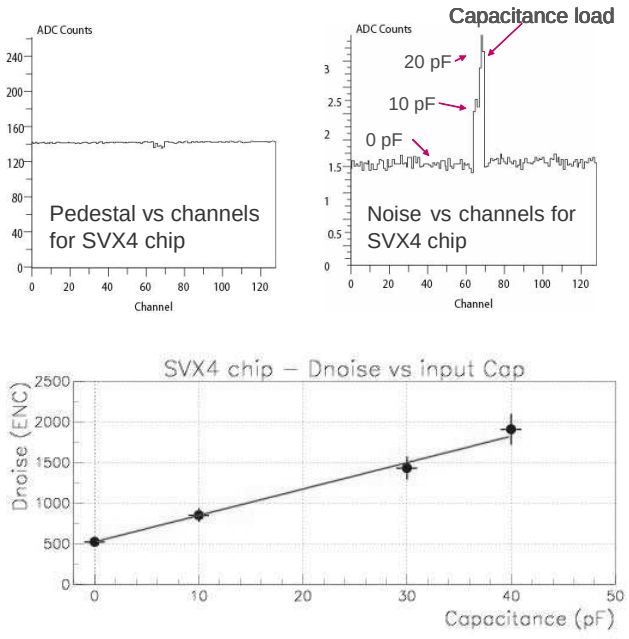

Fig. 8. Pedestal (upper-left) and noise (upper-right) distribution of a single SVX4 chip. Higher noise values for selected channels are due to different capacitive loads. The lower plot shows noise versus input capacitive load.

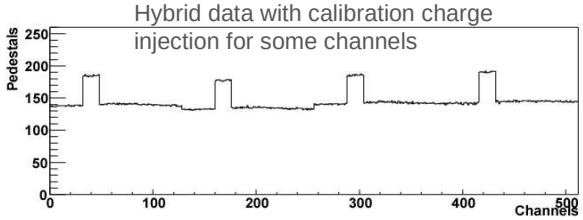

Fig. 9. Hybrid pedestal distribution. Charge is injected on selected channels.

B. Stave testing

It is very important to retain this excellent noise performance also on a stave. This is not so trivial as the bus cable, running directly underneath the silicon sensors, is constantly busy with clocks, controls and data signals while the front end is acquiring data. For this reason a 25 μm thick Al shield is added to the bus cable. This proved quite effective in shielding the sensors from activity on the bus. Extensive studies on proper grounding of the bus cable shield, carbon fibers support structure, and sensors high voltage reference have been performed before reaching a final configuration on the stave. We found that optimal performance are reached when the sensors high voltage line is reference to analog ground on the hybrid, the bus cable shield is broken under each module and grounded separately to analog ground also on the hybrid directly above and the carbon fiber structure grounded to the Mini Port Card ground at one end of the stave. Noise (blue) and differential noise (red) distribution is given for a full stave in figure 10 (top). Noise on the stave is around 1,200 electrons as the typical gain for the preamps is about 500 electrons per ADC. Dead-timeless performance are a key issue for stave operation at CDF. Studies to date indicate acceptable performance [10].

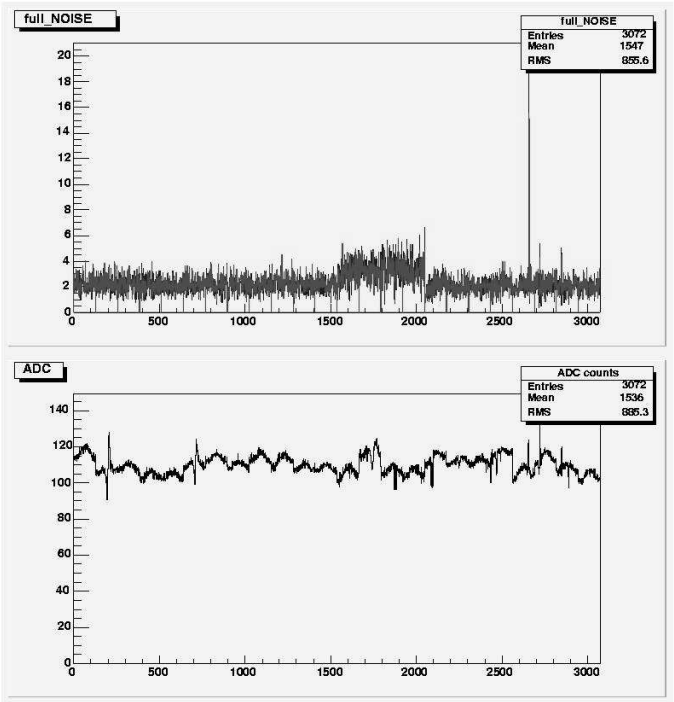

Fig. 10. Noise (top, blue), dnoise (top, red) and pedestal (bottom) distribution for a full stave. A total of 3072 channels are readout. Noise and dnoise coincides (i.e. no common mode noise) with a value of ~ 1,200 electrons. The slightly higher noise between channels 1536 to 2048 are due to a different gain setting on that particular module. The bow-shaped pedestal on a chip by chip basis visible in the pedestal distribution has been corrected on the preproduction submission of the SVX4 chip (see ref. [11]).

C. Laser Run on Stave

Stave performance was also studied using a 1064 nm focused laser signal. The offline pedestal subtracted data, as shown in

the Figure 11, has a clear and clean laser signal covering a few strips.

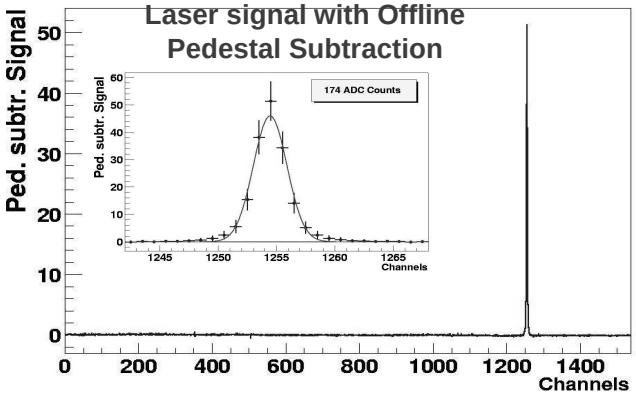

Fig.11. Offline pedestal subtracted laser data. A clear signal is seen around channel 1255 in the area illuminated by the laser.

V. SUMMARY AND PLAN

Although the SVXIIb project has been recently terminated due to revised Tevatron luminosity plans, we are proceeding with a closed out plan of the project as silicon sensors, SVX4 chips and hybrids are already available in preproduction quantities. About 15 staves and 4 L0 modules will be built and installed on prototype barrel and L0 carbon fiber support structure respectively. The L0 support structure will be inserted into the barrel and system testing will be performed using this configuration to demonstrate the feasibility of the SVXIIb design.

VI. REFERENCE

[1] CDF Collaboration, 'the Run IIb Technical Design Report', CDF-NOTE 6261.

[2] M. Aoki, *et al*, 'The CDF Run IIb Silicon Detector', CDFNOTE 6750, to be published in the proceeding of Frontier Detectors for Frontier Physics, Isola d'Elba, Italy, May 25-31, 2003.

[3] J.Antos et al.,'The SVXII silicon detector upgrade at CDF', Nucl. Inst. and Meth. A383:13-20, 1996

[4] C.Hill 'Initial experience with the CDF Layer 00 silicon detector', Nucl. Inst. and Meth. A511:118-120, 2003

[5] B.Krieger *et al*. 'SVX4: a new deep submicron readout IC for the Tevatron collider at Fermilab', to be published in the proceeding of IEEE Nuclear Science Symposium 2003, Portland, Oregon, U.S.A. Oct. 19-25, 2003.

[6] A.Affolder et al., 'Intermediate silicon layers detector for the CDF experiment', Nucl. Inst. and Meth. A453:84-88, 2000

[7] K.Burkett, 'Design and construction of the CDF central outer tracker', Nucl. Inst. and Meth. A461:62-64, 2001

[8] R.J.Tesarek et. al., 'A measurement of the radiation environment in the CDF tracking volume', Nucl. Inst. and Meth. A514:188-193, 2003

[9] K.Hara *et al*. 'Silicon sensor quality assurance for the CDF RunIIb Silicon detector', CDF-NOTE 6283

[10] M. M. Weber, 'Electrical Performance and Dead-timeless Operation of "Staves" for the New CDF Silicon Detector', to be published in the proceeding of IEEE Nuclear Science Symposium 2003, Portland, Oregon, U.S.A. Oct. 19-25, 2003.

[11] M.Garcia-Sciveres et. al., 'The SVX4 integrated circuit', Nucl. Inst. and Meth. A511:171-173, 2003